AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 1, 3, and 5-10 as shown below.

The following is a complete list of all claims in this application.

1. (Currently Amended) A thin film transistor array substrate for a liquid crystal display, comprising:

an insulating substrate ~~with~~ including a display area and a peripheral area surrounding the display area, the peripheral area ~~having~~ including an upper region arranged above the display area and a lower region arranged below the display area;

signal lines formed on the insulating substrate ~~such~~, wherein ~~that~~ the signal lines are bundled into a plurality of blocks, each block ~~having~~ including a predetermined number of signal lines;

a plurality of first upper repair lines formed ~~at~~ in the upper ~~peripheral~~ region of the substrate, wherein the plurality of first upper repair lines ~~crossing~~ cross one or more ~~blocks~~ of the plurality of blocks ~~signal lines~~;

a plurality of second upper repair lines formed ~~at~~ in the upper ~~peripheral~~ region of the substrate, wherein the second upper repair lines cross ~~crossing~~ all of the signal lines;

a plurality of first lower repair lines formed at the lower ~~peripheral~~ region of the substrate, connected to the corresponding first upper repair lines, wherein the first lower repair lines cross ~~crossing~~ the signal lines crossed by the first upper repair lines;

a plurality of second lower repair lines formed at the lower ~~peripheral~~ region of the substrate, wherein the plurality of second lower repair lines cross ~~crossing~~ all of the signal lines;

a plurality of upper connection members crossing the first upper repair lines and the second upper repair lines; and

a plurality of lower connection members crossing the first lower repair lines and the second lower repair lines.

2. (Original) The thin film transistor array substrate of claim 1, further comprising:

a plurality of first interconnection lines interconnecting the first upper repair lines and the first lower repair lines.

3. (Currently Amended) The thin film transistor array substrate of claim 2, wherein the first upper repair lines extend ~~are drawn~~ from two or more dummy pins of integrated circuits for driving the signal lines, and are ~~linked~~ coupled to the first interconnection lines.

4. (Original) The thin film transistor array substrate of claim 2, further comprising:

a plurality of second interconnection lines interconnecting the first upper repair lines and the first lower repair lines.

5. (Currently Amended) The thin film transistor array substrate of claim 1, further comprising:

a plurality of third upper repair lines formed at the upper ~~peripheral~~ region of the substrate while crossing the upper connection members and all of the signal lines; and

a plurality of third lower repair lines formed at the lower ~~peripheral~~ region of the substrate while crossing the lower connection members and all of the signal lines.

6. (Currently Amended) The thin film transistor array substrate of claim 1, wherein each block of the signal lines comprises the signal lines connected to ~~one of the~~ an integrated circuit ~~circuits~~.

7. (Currently Amended) The thin film transistor array substrate of claim 6, wherein the first upper line and the first lower repair ~~lines~~ line cross two blocks of the signal lines.

8. (Currently Amended) The thin film transistor array substrate of claim 7, wherein one or more of the upper connection member and the lower connection ~~members~~ member are formed at each block of the signal lines.

9. (Currently Amended) The thin film transistor array substrate of claim 4, wherein the first interconnection line and the second interconnection ~~lines~~ line are formed on a printed circuit board.

10. (Currently Amended) The thin film transistor array substrate of claim 4, further comprising:

a signal amplifying circuit in the first interconnection line and the second interconnection ~~lines~~ line.